Multi-Die Polylithic Integration Enabled by Heterogeneous Interconnect Stitching Technology (HIST)

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***Abstract*—In this paper, a multi-die polylithic integration approach using Heterogeneous Interconnect Stitching Technology (HIST) is explored for low-loss, high-density, and low-energy electronic systems. In the HIST approach, stitch-chips, which are either active or passive, are used for such signal pathways between assembled 'anchor chips,' while surface-embedded chips utilize 3D face-to-face electrical interconnections. Fine-pitch and multi-height Compressible MicroInterconnects (CMIs) are used to provide low-loss and mechanically robust interfaces between the anchor chips and the stitch-chips as well as the surface-embedded chips. Electrical measurements of the assembled chips are reported and demonstrate robust interconnection. EM simulations show that low-loss signal interconnection (< -0.4 dB) can be achieved by using 90 µm tall CMIs and 500 µm long channels on quartz stitch-chips.**

Keywords—Heterogeneous integration, Polylithic integration, Compliant interconnects

I. INTRODUCTION

The explosive growth in the mobile and telecommunication markets, autonomous vehicles, Artificial Intelligence (AI), and big data has pushed the semiconductor industry towards ever more complex and sophisticated chip designs. During the last few decades, this has been enabled by forming a monolithic System-on-Chip (SoC) through silicon technology scaling [1]. However, as Moore's Law approaches its limits, this has led to a progressive rise in design time and fabrication cost in advanced silicon technologies with potential yield challenges for large die [2], [3]. As such, it is becoming clear that future high-performance electronics will progressively rely more on advanced heterogeneous system integration (for example, 2.5D and 3D IC technologies) in order to meet cost, performance, and energy requirements. For example, AMD and GLOBALFOUNDRIES have reported approximately 40% and 63% reduction in fabrication costs by partitioning a large monolithic die into multiple smaller dice owing to increased die yield [2], [3].

In this paper, we describe a Heterogeneous Interconnect Stitching Technology (HIST) to enable ***ultimate flexibility*** in polylithic multi-die integration yet yield monolithic-like performance, low manufacturing cost, low-loss signal interconnection, and high-density integration of electronic

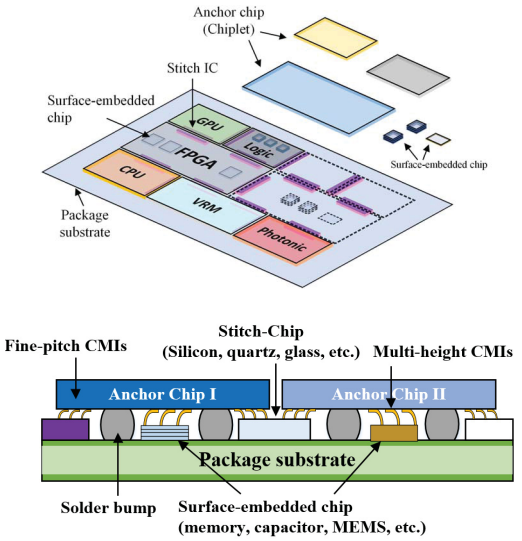

Fig. 1. Schematic of the HIST platform enabled by CMIs for polylithic multi-die integration

systems [4]. Fig. 1 illustrates a schematic of the proposed integration platform. In the simplest form, stitch-chips with dense interconnects are placed between the package substrate and the 'anchor chips' to form a concatenated electronic system. Fine-pitch Compressible MicroInterconnects (CMIs) are used to provide high-bandwidth signal interfaces between the anchor chips through the stitch-chips. Multi-height CMIs are used to enable interconnections between the anchor chips and the 'surface-embedded chips.' Power delivery and signal I/Os to the package substrate can be formed using multi-height CMIs or solder bumps. Mechanical bonding between the anchor chips and the package substrate is formed using large solder bumps to help reworkability of assembled die. The stitch-chips, in the simplest form as noted earlier, provide such signal pathway between the anchor chips, yet the stitch-chips can also contain high-quality passives and/or active circuits. The anchor chips may be ASIC, CPU, GPU, FPGA, MMIC, or photonic die, and the surface-embedded chips may be a decoupling capacitor, memory die, MEMS die, or an Integrated Passive Device (IPD) die, for example. Since CMIs are elastically compressible unlike conventional solder bumps, HIST can compensate for any possible off-chip interconnection length differences resulting from chip thickness differences or

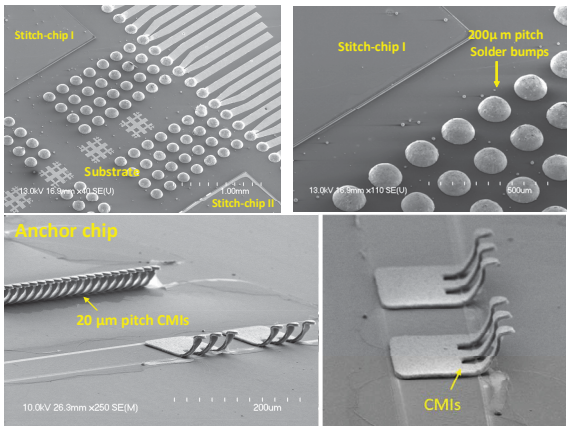

Fig. 2. SEM images of the fabricated solder bumps and fine-pitch (20 µm in-line pitch) CMIs

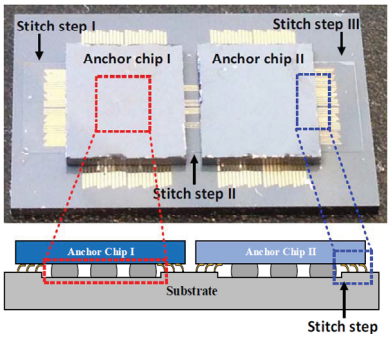

Fig. 3. Optical image of the assembled testbed

chips manufactured from different vendors; this enables face-to-face direct interconnection of dice while maintaining low-system footprint. In addition to this, HIST may have improved thermomechanical reliability owing to the compliance of the CMIs; this is key as it affords designers greater flexibility in the use of various substrate materials, such as silicon, quartz, GaN, InP, and GaAs, for example. Eliminating (or at least greatly minimizing) the constraints in chip thickness variations and substrate materials and ability to enabled both 2.5D and 3D face-to-face interconnection all using one platform are key and unique advantages that HIST provides; such new design freedoms unlock new digital and mm-wave architectures that may be challenging with conventional interconnect solutions.

II. Fabrication and Assembly of HIST Platform

In order to demonstrate the key features of the HIST platform, an experimental testbed is fabricated, assembled, and tested. Anchor chips with fine-pitch CMIs are assembled onto a silicon substrate containing structures emulating multi-height stitch-chips. In this testbed, the stitch-chips on the package substrate are emulated using 20 µm tall steps on the silicon substrate. Fig. 2 shows SEM images of the fabricated silicon substrate containing solder bumps and multi-height steps to emulate multi-thickness stitch-chips. The fabricated fine-pitch CMIs are approximately 40 µm in height and formed on a 20 µm in-line pitch while the solder bumps are approximately 50 µm in height and 200 µm in pitch. The fine-pitch CMIs provide high I/O density for signaling between the anchor chips and the stitch-chips; their unique upward curved

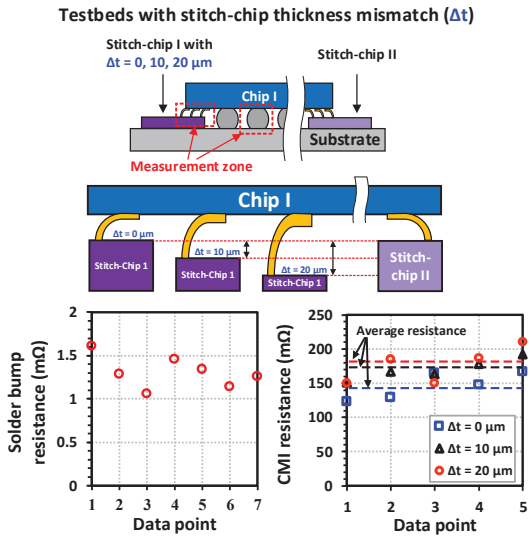

Fig. 4. Four-point resistance measurement results of the fabricated solder bumps and fine-pitch CMIs

geometry ensures that their tips remain in contact with the receiving pad during assembly. CMI fabrication details are described in [5].

Optical image of the assembled testbed is shown in Fig. 3. A Finetech Lambda flip-chip bonder was used for assembly. The two anchor chips in Fig. 3 are placed side-by-side onto three 'stitch-chips.' The solder bumps are reflowed after the anchor chips are aligned to the silicon substrate; the reflowed solder bumps provide electrical and mechanical interconnection to the substrate. The mechanical interconnection (of the solder bumps) forms and maintains the compressive force on the CMIs, which is needed for robust low-resistance interconnection. As shown in Fig. 3, the center of the anchor chip is bonded to the silicon substrate using solder bumps, while two edges of the chip are suspended above the silicon steps and supported by the fine-pitch CMIs. Fabrication details of multi-height CMIs are reported in [6].

III. Experimental and Simulation Characterization

Following the assembly, the four-point resistances of the interconnections were measured using a Karl-Suss probe station. In order to demonstrate the multi-height face-to-face interconnections, three substrates containing different stitch-chip thickness mismatches (Δt = 0 µm, 10 µm, and 20 µm) were used for anchor chip assembly, as shown in Fig. 4. The resistances of the fine-pitch CMIs in contact with the gold pads on the 'stitch-chips' were measured. The reflowed solder bumps were also measured. As shown in Fig. 4, the average resistance of the CMIs, including contact resistance, is 146.31 mΩ, 170.02 mΩ, and 176.71 mΩ, respectively for Δt = 0 µm [i.e., thicker stitch-chip], 10 µm, and 20 µm [i.e., thinner stitch-chip]. The average resistance of the solder bumps is 1.31 mΩ. These four-point resistance measurement results confirm that the CMIs maintain electrical connections between the anchor chip and the stitch-chips even as the CMIs are compressed by different gaps which represent stitch-chip thickness differences that may result from heterogeneous stitch-chips (manufactured using different processes and/or materials).

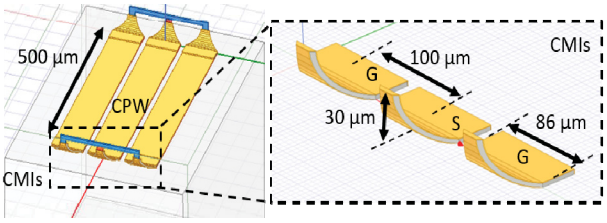

Fig. 5. Schematic of HFSS model of a quartz stitch-chip.

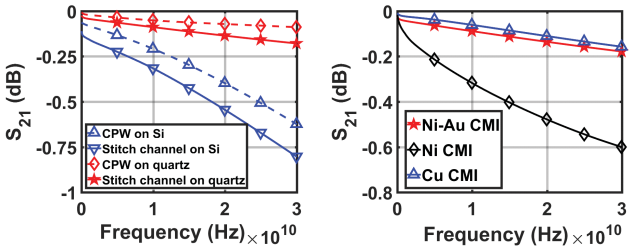

Fig. 6. Insertion loss (S_{21}) of stitch-chip channel (a) with different substrate materials and (b) with different CMIs materials

EM simulations, using HFSS, were performed to demonstrate low-loss interconnection through the stitch-chip using CMIs. Since the stitch-chip can be formed using a variety of substrate materials depending on application, stitch-chip using quartz substrate was used for the EM simulations as an example and due to its low-substrate loss, which is key in high-speed digital and mm-wave transmission. Fig. 5 illustrates a quartz stitch-chip with Coplanar Waveguides (CPWs) and CMIs. The CPW is 3 µm thick copper and the CMIs are assumed to be nickel-core with 500 nm thick gold coating on the surface. The CPW's characteristic impedance (Z_0) is 50 Ω.

First, in order to investigate the effects of different substrate materials on the insertion loss, S_{21} was simulated up to 30 GHz using high-resistivity silicon (1 kΩ • cm) and quartz substrate, as shown in Fig. 6 (a). The dimensions of CPWs are modified to achieve a Z_0 of 50 Ω. The simulated CPW on quartz substrate shows approximately -1.4 dB/cm loss at 20 GHz, which is close to the loss of CPW on quartz substrate reported in [7]. The CPW on silicon substrate results in higher insertion loss compared to that on quartz. Another important material selection is that of the CMIs. In the demonstrated experiments in the previous section, the CMI core is formed using a nickel alloy (NiW) for mechanical properties principally while the outer layer is formed using gold to prevent oxidation and reduce resistance (DC and AC) [8]. To investigate the impact of various relevant materials on CMI performance, the model in Fig. 5 was used again. As shown in Fig. 6 (b), the stitch-chip channel with copper CMIs shows the lowest insertion loss compared to other materials owing to the higher conductivity and larger skin depth at high frequency. The stitch-chip channel with nickel CMIs (to represent NiW) has higher insertion loss. However, the gold coated Ni-based CMIs show improvement since the majority of the current distribution concentrates within the gold layer (higher conductivity and larger skin depth) due to the skin effect at high frequency. Next, a stitch-chip channel with CMIs of different heights, including 30 µm, 60 µm, and 90 µm, were simulated. As can be seen from Fig. 7, the height of

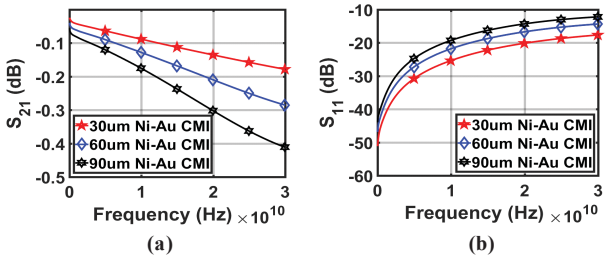

Fig. 7. S-parameters of stitch-chip channel with CMIs of different heights

CMIs minimally increases the loss due to their small form factor.

IV. Conclusion

This paper explores the fabrication and assembly processes of HIST platform featuring CMIs. Experimental characterization of the HIST platform was performed by assembling a testbed with fine-pitch CMIs and solder bumps, and the results show that CMIs can enable robust electrical interconnection between the concatenated anchor chips irrespective of any possible stitch chip thickness differences. These results demonstrate a new degree of freedom in system-level integration flexibility when compared to conventional microbumps. The simulation results show that stitch-chips using quartz substrate are promising for low-loss signal interconnection, which is crucial in high-performance computing applications. No through-substrate-vias are utilized in the proposed research.

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